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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

	Application Number	09/483,712
	Filing Date	January 14, 2000
	First Named Inventor	Jiang et al.
	Group Art Unit	2815
	Examiner Name	M. Warren
	Attorney Docket Number	2269-3815.1US (98-0670.00/US)

ENCLOSURES (check all that apply)

<input checked="" type="checkbox"/> Postcard receipt acknowledgment (attached to the front of this transmittal)	<input type="checkbox"/> Information Disclosure Statement, PTO/SB/08A (08-00); <input type="checkbox"/> copy of cited references	<input type="checkbox"/> Terminal Disclaimer
<input checked="" type="checkbox"/> Duplicate copy of this transmittal sheet in the event that additional filing fees are required under 37 C.F.R. § 1.16	<input type="checkbox"/> Supplemental Information Disclosure Statement; PTO/SB/08A (08-00); copy of cited references and Check No. in the amount of \$180.00	<input type="checkbox"/> Terminal Disclaimer
<input type="checkbox"/> Preliminary Amendment	<input type="checkbox"/> Associate Power of Attorney	<input type="checkbox"/> Terminal Disclaimer
<input type="checkbox"/> Response to Restriction Requirement/Election of Species Requirement dated	<input type="checkbox"/> Petition for Extension of Time and Check No. in the amount of \$	
<input type="checkbox"/> Amendment in response to office action dated	<input checked="" type="checkbox"/> Petition to Withdraw Holding of Abandonment Pursuant to 37 C.F.R. § 1.181	
<input type="checkbox"/> Amendment under 37 C.F.R. § 1.116 in response to final office action dated	<input type="checkbox"/> Fee Transmittal Form	
<input type="checkbox"/> Additional claims fee - Check No. in the amount of \$	<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> Other Enclosure(s) (please identify below):
<input type="checkbox"/> Letter to Chief Draftsman and copy of FIGS. with changes made in red	<input type="checkbox"/> Assignment Papers (for an Application)	
<input type="checkbox"/> Transmittal of Formal Drawings	<div style="border: 1px solid black; padding: 2px;">Remarks</div>	
<input type="checkbox"/> Formal Drawings (sheets)	<p>The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.</p>	

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

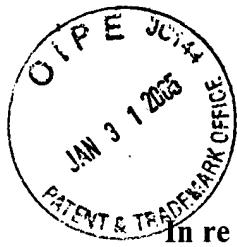
Firm or Individual name	Joseph A. Walkowski	Registration No. 28,765
Signature		
Date	January 31, 2005	

CERTIFICATE OF MAILING

Express Mail Label Number: EL994823949US

Date of Deposit: January 31, 2005

Person Making Deposit: Steve Wong



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jiang et al.

Serial No.: 09/483,712

Filed: January 14, 2000

For: CHIP-SCALE PACKAGES HAVING
ENCAPSULATED CARRIER BONDS

Confirmation No.: 8743

Examiner: M. Warren

Group Art Unit: 2815

Attorney Docket No.: 2269-3815.1US
(98-0670.00/US)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL994823949US

Date of Deposit with USPS: 1/31/2005

Person making Deposit: Steve Wong

**PETITION TO WITHDRAW HOLDING OF ABANDONMENT
PURSUANT TO 37 C.F.R. §1.181**

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby petition the Commissioner of Patents and Trademarks to invoke the supervisory authority of the Commissioner, pursuant to 37 C.F.R. §1.181, to withdraw the Office's holding of abandonment in the above-captioned patent application.

STATEMENT OF FACTS AND POINTS TO BE REVIEWED

On **November 19, 2004**, the Patent Office mailed an adverse Decision on Appeal of the Board of Patent Appeals and Interferences in the above-captioned patent application. On **January 12, 2005**, Applicants responded, by Express Mail, by filing a Request for Continued Examination (RCE) and Amendment Accompanying Request for Continued Examination (RCE with the required fee, pursuant to 37 CFR 1.114 and 37 CFR 1.17(e) to reopen prosecution in the application in accordance with M.P.E.P. 1214.07.

Applicants then received a Notice of Abandonment with a mailing date of January 19, 2005. The Notice of Abandonment lists the reason for abandonment as "The decision by the Board of Patent Appeals and Interference rendered on 19 November 2004 and because the period for seeking court review of the decision has expired and there are no allowed claims." In accordance with M.P.E.P. 1214.06, the Office should not have issued a Notice of Abandonment until the time for seeking court review (two (2) months under 37 CFR 1.304) plus two (2) weeks had expired.

In the present situation, Applicants filed an RCE with an appropriate Amendment and required fee in a timely manner BY Express Mail less than two (2) months after the Decision on Appeal. Accordingly, the holding of abandonment by the Office is inappropriate and in error, and should be withdrawn.

A copy of the Notice of Abandonment with a mailing date of January 19, 2005 is enclosed. Also enclosed are copies of documents filed January 12, 2005, including: Request for Continued Examination (RCE) Transmittal; Check no. 7256 in the amount of \$790.00; and Amendment Accompanying Request for Continued Examination (RCE). Additionally, a copy of the date-stamped return postcard evidencing receipt of the foregoing documents as well as a receipt date by the Office of January 12, 2005 is enclosed.

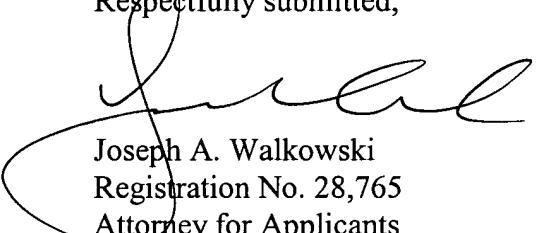
No fee for this petition to the Commissioner is required under 37 C.F.R. 1.181(d), as indicated by MPEP §711.03(c).

Applicants respectfully submit that this petition is timely filed, as the Notice of Abandonment was mailed by the Patent Office on November 19, 2004, the Request for Continued Examination (RCE) documents were mailed on January 12, 2005 by Express Mail, and Applicants have filed this petition within two months of the mailing date of the Notice of Abandonment.

RELIEF REQUESTED

Applicants respectfully request that this petition be granted and the holding of abandonment be withdrawn promptly, the request for Continued Examination (RCE) and Amendment Accompanying Request for Continued Examination (RCE) be entered herein, prosecution of this matter before the Examiner be reopened and an Office Action on the merits issued in a timely manner.

Respectfully submitted,



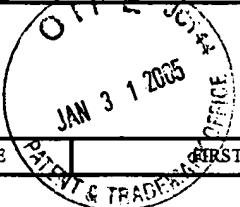
Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: January 31, 2005
JAW/dlm:ljb

Document in ProLaw



UNITED STATES PATENT AND TRADEMARK OFFICE



UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/483,712	01/14/2000	Tongbi Jiang	3815US (98-0670)	8743

7590 01/19/2005

Joseph A Walkowski
TRASK BRITT & ROSSA
P O Box 2550
Salt Lake City, UT 84110

RECEIVED

JAN 20 2005

TRASKBRITT, P.C.

EXAMINER

WARREN, MATTHEW E

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 01/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.



Notice of Abandonment	Application No.	Applicant(s)
	09/483,712	JIANG ET AL.
	Examiner	Art Unit
	Matthew E Warren	2815

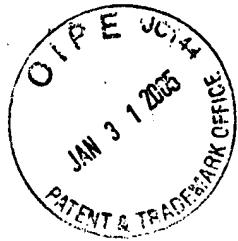
-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. Applicant's failure to timely file a proper reply to the Office letter mailed on _____.
(a) A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
(b) A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 (a) to the final rejection.
(A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
(c) A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
(d) No reply has been received.
2. Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
(a) The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
(b) The submitted fee of \$_____ is insufficient. A balance of \$_____ is due.
The issue fee required by 37 CFR 1.18 is \$_____. The publication fee, if required by 37 CFR 1.18(d), is \$_____.
(c) The issue fee and publication fee, if applicable, has not been received.
3. Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
(a) Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
(b) No corrected drawings have been received.
4. The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.
5. The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.
6. The decision by the Board of Patent Appeals and Interference rendered on 19 November 2004 and because the period for seeking court review of the decision has expired and there are no allowed claims.
7. The reason(s) below:

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2000

Petitions to revive under 37 CFR 1.137(a) or (b), or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.



THE PATENT & TRADEMARK OFFICE MAILROOM DATE
STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS
DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Request for Continued Examination (RCE) Transmittal (1 page,
w/duplicate copy); Check no. 7256 in the amount of \$790.00; and
Amendment Accompanying Request for Continued Examination (RCE).

Invention: CHIP-SCALE PACKAGES HAVING
ENCAPSULATED CARRIER BONDS
Applicant(s): Jiang et al.
Filing Date: January 14, 2000
Serial No.: 09/483,712
Date Sent: January 12, 2005 via Express Mail Label No.
Docket No.: EL994824051US
JAW/dlm:jb

7256
TRASK BRITT, P.C. PATENT ATTORNEYS / CLIENT ADVANCE ACCOUNT

DATE	INVOICE #	REFERENCE	AMOUNT
01/12/2005		Request for continued examination (RCE) 2269-3815.1U9	790.00
			790.00

WARNING THIS DOCUMENT HAS FLUORESCENT FIBERS. A VOID PANTOGRAPH AND A MICROPRINT SIGNATURE LINE

7256
TRASK BRITT, P.C.
PATENT ATTORNEYS / CLIENT ADVANCE ACCOUNT
230 SOUTH 500 EAST, SUITE 300
P.O. BOX 2550
SALT LAKE CITY, UT 84102
PHONE: 801-532-1922

KEY BANK OF UTAH
SALT LAKE CITY, UT
31-7371240

DATE 01/12/2005

PAY
EXACTLY

Seven Hundred Ninety AND 00/100 DOLLARS.

TO THE
ORDER OF

Commissioner for Patents
Washington, D.C. 20231

AUTHORIZED SIGNATURE

1017256 240007371445010030416

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**REQUEST
FOR
CONTINUED EXAMINATION (RCE)
TRANSMITTAL**

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	09/483,712
Filing Date	January 14, 2000
First Named Inventor	Jiang et al.
Art Unit	2815
Examiner Name	M. Warren
Attorney Docket Number	2269-3815.1US (98-0670.00/US)

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application. Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 C.F.R. 1.114

a. Previously submitted

- Consider the amendment(s)/reply under 37 C.F.R. 1.116 previously filed on _____
(Any unentered amendment(s) referred to above will be entered).
- Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- Other _____

b. Enclosed

- Amendment/Reply
- Affidavit(s)/Declaration(s)
- Information Disclosure Statement (IDS)
- Other _____

2. Miscellaneous

a. Suspension of action on the above-identified application is requested under 37 C.F.R. 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. 1.17(i) required)

b. Other _____

3. Fees The RCE fee under 37 C.F.R. 1.17(e) is required by 37 C.F.R. 1.114 when the RCE is filed.

a. The Director is hereby authorized to charge any deficiency in the following fees, or credit any overpayments, to Deposit Account No. 20-1469

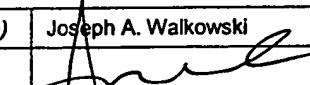
- RCE fee required under 37 C.F.R. 1.17(e)
- Extension of time fee (37 C.F.R. 1.136 and 1.17)
- Other _____

b. Check in the amount of \$790.00 enclosed

c. Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print /Type)	Joseph A. Walkowski	Registration No. (Attorney/Agent)	28,765
Signature		Date	January 12, 2005

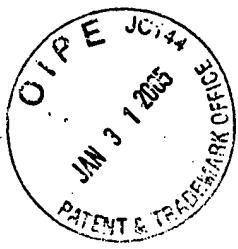
CERTIFICATE OF MAILING

Express Mail Label Number: EL994824051US

Date of Deposit: January 12, 2005

Person Making Deposit: Steve Wong

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND Fees and Completed Forms to the following address: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jiang et al.

Serial No.: 09/483,712

Filed: January 14, 2000

For: CHIP-SCALE PACKAGES HAVING
ENCAPSULATED CARRIER BONDS

Confirmation No.: 8743

Examiner: M. Warren

Group Art Unit: 2815

Attorney Docket No.: 2269-3815.1US
(98-0670.00/US)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL994824051US

Date of Deposit with USPS: January 12, 2005

Person making Deposit: Steve Wong

AMENDMENT ACCOMPANYING REQUEST FOR
CONTINUED EXAMINATION (RCE)

Mail Stop RCE
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

This Amendment is submitted simultaneously with a REQUEST FOR CONTINUED EXAMINATION. Prior to examination of the above-referenced patent application on the merits, entry of the amendments as set forth herein is respectfully solicited.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

Amendments to the Claims:

Claims 1 through 20 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A chip-scale package comprising:

a semiconductor die having an active surface having at least one bond pad thereon, sides and a back side;

at least one conductive trace-lead frame member laterally spaced from said the at least one bond pad and having an upper surface and a lower surface, the lower surface of said the at least one conductive trace-lead frame member having and inner end and an outer end and being substantially non-conductively attached to a portion of the active surface of said the semiconductor die and vertically spaced therefrom by a non-coextensive dielectric element interposed therebetween;

at least one discrete conductive bond connecting the inner end of the at least one conductive trace-lead frame member to the at least one bond pad on the active surface of said the semiconductor die;

at least one carrier bond directly attached to the upper surface of the at least one conductive tracelead frame member at the outer end thereof and extending transversely thereto; and an encapsulant material disposed between the active surface of the semiconductor die and a portion of the lower surface of the at least one conductive lead frame member, extending over encapsulating said the sides and the back side of the semiconductor die, the outer end of the at least one conductive tracelead frame member, the at least one discrete conductive bond and a portion of the at least one carrier bond, the at least one carrier bond having including another portion extending beyond said an outer surface of the encapsulant material.

2. (Currently Amended) A chip-scale package comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon;
a dielectric element having an upper surface and a lower surface, the lower surface of said the dielectric element attached to a portion of the active surface of said the semiconductor die;
a plurality of conductive traces lead frame members having inner ends laterally spaced from said the plurality of bond pads, each trace-conductive lead frame member of the plurality of conductive traces lead frame members having an upper surface and a lower surface, a portion of the lower surface of each trace-conductive lead frame member of said the plurality of conductive traces lead frame members being attached to a portion of the upper surface of said the dielectric element for connecting each conductive trace-lead frame member of said the plurality of conductive traces lead frame members to the active surface of said the semiconductor die;
a plurality of discrete conductive bond members, at least one discrete conductive bond member of the plurality of conductive bond members connecting the inner end of each conductive trace-lead frame member of said the plurality of conductive traces lead frame members to at least one bond pad of the plurality of bond pads on the active surface of said the semiconductor die;
a plurality of conductive carrier bonds, at least one carrier bond of the plurality of conductive carrier bonds directly disposed on the upper surface of each conductive trace-lead frame member of said the plurality of conductive traces lead frame members at a location remote from the inner end thereof and extending transversely from the upper surface thereof; and
an encapsulating material disposed about at least portions of said the semiconductor die, about said the dielectric element, between the active surface of the semiconductor die and the lower surface of a portion of each lead frame member of the said plurality of conductive traces lead frame members, over outer ends of the lead frame members of the plurality, over said the plurality of discrete conductive bond members and over a portion of each carrier bond of said the plurality of conductive carrier bonds, another portion of each carrier bond extending beyond an outer surface of the encapsulating material.

3. (Currently Amended) A chip-scale package as in claim 2, wherein said-the dielectric element includes an adhesive-coated polyimide tape.

4. (Currently Amended) A chip-scale package as in claim 2, wherein said-the dielectric element includes a polyimide film.

5. (Currently Amended) A chip-scale package as in claim 2, wherein the upper surface and lower surface of said-the dielectric element are attached respectively to a portion of the lower surface of each conductive trace-lead frame member of said-the plurality of conductive traces lead frame members and a portion of the active surface of said-the semiconductor die connecting portions of said-the plurality of conductive traces-lead frame members and to portions of said-the active surface of the semiconductor die.

6. (Currently Amended) A chip-scale package as in claim 2, wherein said-the plurality of conductive traces-lead frame members comprises a plurality of lead fingers.

7. (Currently Amended) A chip-scale package as in claim 2, wherein said-the plurality of conductive traces-lead frame members comprises a conductive metal.

8. (Currently Amended) A chip-scale package as in claim 2, wherein said-the plurality of discrete conductive bond members comprises a conductive metal.

9. (Currently Amended) A chip-scale package as in claim 2, wherein said-the plurality of discrete conductive bond members comprises bond wires.

10. (Currently Amended) A chip-scale package as in claim 9, wherein said-the bond wires comprise gold or aluminum.

11. (Currently Amended) A chip-scale package as in claim 2, wherein said-the plurality of discrete conductive bond members comprises TAB bonds.

12. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~the plurality of discrete conductive bond members comprises thermocompression bonds.

13. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~the plurality of conductive carrier bonds includes metal.

14. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~the plurality of conductive carrier bonds comprises a conductive or conductor-filled polymer.

15. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~the plurality of conductive carrier bonds is selectively located on the upper ~~surface~~surfaces of ~~said~~the plurality of conductive ~~traces~~lead frame members, forming an array over the active surface of the semiconductor die.

16. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~the plurality of conductive carrier bonds comprises solder balls.

17. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~the encapsulating material comprises a substantially non-conductive material.

18. (Currently Amended) A chip-scale package as in claim 2, wherein ~~said~~the encapsulating material comprises a material having a low modulus of elasticity.

19. (Currently Amended) A chip-scale package as in claim 2, wherein each conductive carrier bond of ~~said~~the plurality of conductive carrier bonds further comprises an upper portion and a lower portion, ~~said~~the lower portion of ~~a~~each conductive carrier bond being attached to the upper surface of ~~a~~an associated conductive ~~trace~~lead frame member of ~~said~~the plurality of conductive ~~traces~~lead frame members.

20. (Currently Amended) A chip-scale package as in claim 19, wherein said the encapsulating material is disposed only about the lower portions of said the plurality of conductive carrier bonds.

21. (Withdrawn) A method for fabricating a chip-scale package comprising: providing a semiconductor die having an active surface having at least one bond pad disposed thereon; providing at least one conductive trace having an upper surface and a lower surface; dielectrically attaching at least a portion of the lower surface of said at least one conductive trace to a portion of the active surface of said semiconductor die; attaching a conductive bond member between said at least one conductive trace and the at least one bond pad disposed on the active surface of said semiconductor die; attaching at least one carrier bond to a portion of the upper surface of said at least one conductive trace; and encapsulating at least portions of said semiconductor die, said at least one conductive trace, said conductive bond and a portion of said at least one carrier bond.

22. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one conductive trace as a lead frame element.

23. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one conductive trace of a conductive metal.

24. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said conductive bond member as a wire bond.

25. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said conductive bond member as a TAB bond.

26. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one carrier bond as a solder ball.

27. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, further comprising forming said at least one carrier bond comprises an electrically conductive or conductor-filled polymer.

28. (Withdrawn) The method for fabricating a chip-scale package as in claim 21, wherein said dielectrically attaching is effected using a polyimide tape.

29. (Withdrawn) A method for fabricating a chip-sized package as in claim 21, wherein the step of dielectrically attaching at least a portion of the lower surface of said conductive trace to a portion of the active surface of said semiconductor die further comprises: providing a dielectric material having an upper surface and a lower surface; attaching at least a portion of the lower surface of said joint material to at least a portion of the active surface of said semiconductor die; and attaching at least a portion the lower surface of said at least one conductive trace to at least a portion of the upper surface of said joint material.

REMARKS

Claims 1 through 29 are currently pending in the application. Claims 21 through 29 are withdrawn. Claims 1 through 20 have been amended. Applicant respectfully requests reconsideration of the application as amended herein.

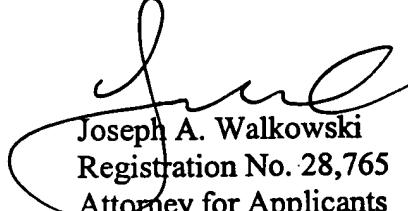
ENTRY OF AMENDMENTS

The amendments to claims 1 through 20 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1 through 20 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



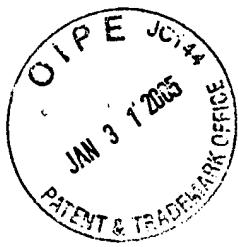
Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicants

TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: January 12, 2005

JAW/dlm:ljb

Document in ProLaw



THE PATENT & TRADEMARK OFFICE MAILROOM DATE
STAMPED THEREON IS AN ACKNOWLEDGEMENT THAT ON THIS
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Amendment Accompanying Request for Continued Examination (RCE).

Invention: CHIP-SCALE PACKAGES HAVING
ENCAPSULATED CARRIER BONDS
Applicant(s): Jiang et al.
Filing Date: January 14, 2000
Serial No.: 09/483,712
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JAW/dlm:ljb

RECEIVED

JAN 24 2005

TRASKBRITT, P.C.

